REMARKS

The indication of allowable subject matter in claims 6-14 is acknowledged and appreciated. In view of the following remarks, it is respectfully submitted that all claims are patentable over the cited prior art.

I. CLAIMS 1-14 ARE DEFINITE

Claims 1-14 stand rejected under 35 U.S.C. § 112, second paragraph. This rejection is respectfully traversed for the following reasons. The Examiner alleges that the use of "not being" in claims 1 and 7 is a negative limitation, whereas claims must be positively recited. It therefore appears that the Examiner has taken the position that negative limitations are *per se* improper. Applicants respectfully disagree. As a preliminary matter, the rejection of claims 1 and 7 is rendered moot by the enclosed amendment which removes the alleged negative limitation. However, newly added claims 22-23 include the "not being" limitation and are submitted to be definite.

The Examiner is directed to MPEP § 2173.05(i), which sets forth the applicable standard:

> The current view of the courts is that there is nothing inherently ambiguous or uncertain about a negative limitation. So long as the boundaries of the patent protection sought are set forth definitely, albeit negatively, the claim complies with the requirements of 35 U.S.C. 112, second paragraph.

In the instant case, it is respectfully submitted that the "boundaries of the patent protection sought [with respect to the limitation 'each of said regions not being involved in electrical connection'] are set forth definitely." Indeed, the Examiner has not asserted otherwise. That is, the Examiner has not indicated specifically why the negative

limitation is indefinite, other than to say it is a negative limitation. As mentioned above, it appears the sole basis of the rejection was the improper assumption that any negative limitation, regardless of whether its metes and bounds are definite, is *per se* improper.

Based on the foregoing, it is respectfully submitted that claims 1-14 are definite. Accordingly, it is respectfully requested that the rejection of claims 1-14 under 35 U.S.C. § 112, second paragraph, be withdrawn.

II. CLAIM 1 IS PATENTABLE OVER ONO ET AL. AND COBBLEY ET AL.

Claim 1 stands rejected under 35 U.S.C. § 103 as being unpatentable over Ono et al. ('551) and Cobbley et al. ('832). This rejection is respectfully traversed for the following reasons. Even assuming *arguendo* proper, the proposed combination does not disclose or suggest the claimed combination.

Claim 1 recites in pertinent part, "a separating/sealing step of separating said semiconductor device from said substrate after heating a bonding place of said adhesive ... if it is determined that said electrical properties are poor in said testing step" (emphasis added). The Examiner admits that Ono et al. does not disclose this feature and therefore relies on Cobbley et al. to modify Ono et al. in an attempt to reach the claimed invention. However, the heating step disclosed by Cobbley et al. is completely unrelated to the testing procedure.

Instead, the heating step of Cobbley et al. is simply used to quick cure the epoxy dots 26 for connecting the dice 28 to the PCB 22 (*see, e.g.,* col. 3, lines 21-23; and Figure 3). That is, rather than heating to soften the adhesive to ease separation, the heating disclosed by Cobbley et al. is expressly used for curing, or hardening, the epoxy to

prevent separation. In fact, col. 6, lines 54-58 (relied on by the Examiner for teaching the heating step) refers to claim 12 of Cobbley et al. which expressly defines the heating step as part of "attaching said at least one IC die to said substrate" (*see* col. 6, lines 45-47).

Once the substrate and IC die are connected, the testing procedure is performed. Turning to the testing procedure, Cobbley et al. is completely silent as to using heating for separating the dice 28 from the PCB 22. Instead, Cobbley et al. discloses generally that "[i]f the assembly 32 fails the test, it is diverted to a rework station, where any [bad] dice 28 ... can easily be removed and reworked" (col. 3, lines 10-13). Cobbley et al. is completely silent as to ***how*** the dice 28 is removed, let alone suggest a heating step therefor.

In this regard, it is respectfully submitted that Cobbley et al., at best, is merely cumulative to the admitted prior art discussed on pages 1-3 of Applicants' specification corresponding to Figure 5. Accordingly, Cobbley et al. is subject to the same drawbacks discussed on page 4, lines 1-3 of Applicants' specification regarding the prior art. Accordingly, the proposed combination fails to disclose or suggest, *inter alia*, "a separating/sealing step of separating said semiconductor device from said substrate after heating a bonding place of said adhesive ... if it is determined that said electrical properties are poor in said testing step" as recited in claim 1.

The Examiner is directed to MPEP § 2143.03 under the section entitled "All Claim Limitations Must Be Taught or Suggested", which sets forth the applicable standard:

> To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (citing *In re Royka*, 180 USPQ 580 (CCPA 1974)).

In the instant case, the pending rejection does not "establish *prima facie* obviousness of [the] claimed invention" as recited in claim 1 because the proposed combination fails the "all the claim limitations" standard required under § 103.

Based on all the foregoing, it is respectfully submitted that claim 1 is patentable over Ono et al. and Cobbley et al.. Accordingly, it is respectfully requested that the rejection of claim 1 under 35 U.S.C. § 103 over Ono et al. and Cobbley et al., be withdrawn.

III. DEPENDENT CLAIMS

Claims 2-4 stand rejected under 35 U.S.C. § 103 over Ono et al., Cobbley et al., and Tsukahara ('093), and claim 5 stands rejected under 35 U.S.C. § 103 over Ono et al., Cobbley et al., and Kohara et al. ('966). These rejections are respectfully traversed for the following reasons.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.,* 819F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 1 is patentable for the reasons set forth above, and because neither Tsukahara nor Kohara et al. were relied on for overcoming the deficiencies of Ono et al. and Cobbley et al., it is respectfully submitted that claims 2-5 which depend on claim 1 are also patentable. In addition, it is respectfully submitted that claims 2-5 are patentable based on their own merits by adding novel and non-obvious features to the combination.

For example, it is respectfully submitted that the proposed combinations are improper because the Examiner has not provided the requisite ***objective*** evidence ***from the prior*** art that suggests the desirability of the proposed combination. The cited prior art does not provide any motivation or rationale for making the proposed combination. The Examiner alleges only that the combination would have been obvious "to enable formation of the adhesive material." However, it is respectfully submitted that Ono et al. equally enables formation of the adhesive material. It is respectfully submitted that merely enabling the formation of the adhesive layer, which is already enabled by Ono et al., is not a sufficient basis for making a modification under § 103.

The Examiner has not identified any rationale or motivation, based on objective evidence from the prior art, that would "suggest the desirability" of ***replacing/modifying*** the adhesive layer of Ono et al. with those disclosed by Tsukahara or Kohara et al.. Simply because Ono et al. can be modified by Tsukahara or Kohara et al. does not make doing so obvious under § 103 without some objective evidence from the prior art that suggests the desirability of the combination (*see* cited MPEP sections below). In the instant case, the cited prior art does not suggest that replacing the adhesive layer of Ono et al. with those disclosed by Tsukahara nor Kohara et al. would be beneficial or desirable.

As is well known in patent law, a *prima facie* showing of obviousness can only be established if the prior art "suggests the desirability" of the proposed combination using objective evidence. The Examiner is directed to MPEP § 2143.01 under the subsection entitled "Fact that References Can Be Combined or Modified is Not Sufficient to Establish *Prima Facie* Obviousness", which sets forth the applicable standard:

> The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. (*In re Mills*, 16 USPQ2d 1430 (Fed. Cir. 1990)).

The Examiner is further directed to MPEP § 2143.01 under the subsection entitled "Fact that the Claimed Invention is Within the Capabilities of One of Ordinary Skill in the Art is Not Sufficient by Itself to Establish *Prima Facie* Obviousness", which sets forth the applicable standard:

> A statement that modifications of the prior art to meet the claimed invention would have been [obvious] because the references relied upon teach that all aspects of the claimed invention were ***individually*** known in the art is ***not*** sufficient to establish a *prima facie* case of obviousness without some objective reason to combine the teachings of the references. (citing *Ex parte Levengood*, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993)).

In the instant case, the Examiner alleges that each of the proposed combinations would have been obvious "to enable formation of the adhesive material." It is submitted that the asserted motivation is *per se* improper because Ono et al. does not need the teachings of Tsukahara or Kohara et al. in order to "enable formation of the adhesive layer" as it can form the adhesive layer without such teachings, and so the Examiner's asserted motivation provides no rationale for making the modification.

Moreover, the Examiner has not indicated why one would ***desire*** modifying Ono et al. with the teachings of Tsukahara or Kohara et al.. Rather, the Examiner simply alleges that one would be capable of doing so. Accordingly, pursuant to the above-cited sections of the MPEP, the cited ***prior art*** does not provide the requisite objective evidence that "suggests the desirability" of the proposed combinations. Only Applicants' specification provides the motivation for making the proposed modifications.

At best, the Examiner has attempted to show only that the elements of the claimed invention are ***individually*** known without providing a *prima facie* showing of obviousness that the ***combination*** of elements recited in the claims is known or suggested in the art. It is therefore submitted that the proposed combination is based solely on improper hindsight reasoning, whereby the Examiner selected bits and pieces of the prior art and used only Applicants' specification as a guide to reconstruct the claimed invention. For all the foregoing reasons, it is submitted that the proposed combinations are improper.

Based on all the foregoing, it is respectfully requested that the rejection of claims 2-5 under 35 U.S.C. § 103 be withdrawn.

IV. NEW CLAIMS

New claims 21-24 are submitted to be patentable based on their own merits by adding novel and non-obvious features to the combination. For example, with respect to claims 22 and 23, neither Cobbley et al. nor Ono et al. disclose or suggest "wherein each of said regions in said bonding step is not involved in an electrical connection."

In contrast, Ono et al. expressly discloses bonding chip 6 to circuit board 9 using conductive adhesives 4,5 in regions which ***are*** involved in electrical connection. That is, conductive adhesives 4,5 electrically connect the electrode pad 3 of the chip 6 to the terminal electrode 8 of the circuit board 9. Similarly, Cobbley et al. discloses bonding dice 28 and PCB 22 together using conductive epoxy dots 26 for making the ***electrical connection*** between the dice 28 and the PCB 22.

V. CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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APPENDIX

IN THE SPECIFICATION

The paragraph beginning on page 10, fifth line from the bottom and ending on page 11, line 15 has been amended as follows:

--First, referring to Fig. 1A, bump electrodes 3 are formed by a known method on electrode pads 2 of an IC board 1 constituting a semiconductor device 4 to form electrical connecting points thereof. Then, an electrically conductive adhesive 7A comprising a thermoplastic resin having a low bonding strength is supplied to either the bump electrodes 3 or input/output terminal electrodes 6 of a circuit board 5 which is a substrate on which the semiconductor device 4 is to be mounted. In Fig. 1A, the electrically conductive adhesive 7A is supplied to the bump electrode 3 side. Further, an adhesive 8A composed of a thermosetting resin having a high bonding strength is supplied to either a region of the semiconductor device 4 which is not involved in electrical connection or a region of the circuit board 5 which is not involved in electrical connection (a rear surface of the semiconductor device 4 or a mounting surface of the circuit board 5). In Fig. 1A, the adhesive is supplied to the semiconductor device 4 side. As a supplying method, an adhesive 8A in a liquid state may be supplied by means of a dispenser or alternatively an adhesive 8A made into a film may be supplied by the transfer method or the like.--

IN THE CLAIMS

1. (Amended) A method of producing a mounting structure comprising:

a connecting step of flip-chip mounting a semiconductor device onto a substrate;

a bonding step of bonding a region of said semiconductor device to a region of said substrate by means of an adhesive[, each of said regions not being involved in electrical connection];

a testing step of performing a test of electrical properties on said semiconductor device and said substrate that are connected to each other; and

a separating/sealing step of separating said semiconductor device from said substrate after heating a bonding place of said adhesive up to a temperature higher than a glass transition point or a melting point of said adhesive if it is determined that said electrical properties are poor in said testing step, and sealing said semiconductor device and said substrate by means of a sealing resin if it is determined that said electrical properties are good in said testing step.

7. (Amended) A method of producing a mounting structure comprising:

a connecting step of flip-chip mounting a semiconductor device onto a substrate;

a bonding step of bonding a region of said semiconductor device to a region of said substrate by means of an adhesive[, each of said regions not being involved in electrical connection];

a peeling permitting layer forming step of forming a peeling permitting layer on an adhesive abutting region of said semiconductor device and/or an adhesive abutting region of said substrate, said peeling permitting layer forming step being performed before said bonding step;

a testing step of performing a test of electrical properties on said semiconductor device and said substrate that are connected to each other; and

a separating/sealing step of separating said semiconductor device from said substrate if it is determined that said electrical properties are poor in said testing step, and sealing a gap between said semiconductor device and said substrate by means of a sealing resin if it is determined that said electrical properties are good in said testing step.